(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 198 085 A1

(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
17.04.2002 Bulletin 2002/16

(21) Application number: **00122026.8**

(22) Date of filing: **10.10.2000**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(51) Int Cl.7: **H04J 3/06**, G06F 1/14

(71) Applicant: **Sony International (Europe) GmbH**
10785 Berlin (DE)

(72) Inventor: **Spalink, Gerd,**
Advanced Technology Center
Hedelfinger Strasse 61, 70327 Stuttgart (DE)

(74) Representative: **Müller . Hoffmann & Partner**
Patentanwälte
Innere Wiener Strasse 17
81667 München (DE)

(54) **Cycle synchronization between interconnected sub-networks**

(57) A method to perform a cycle synchronization between several interconnected sub-networks, comprises the steps that a reference node connected to one of the sub-networks transmits a respective cycle time information to cycle masters of all other sub-networks at recurring time instants, and the cycle masters of all other sub-networks adjust their cycle time accordingly. Therefore, a cycle synchronizator comprises a clock offset estimation means (1) to determine a timing error of an own cycle timer (3), and a cycle adjustment loop (2) receiving the timing error determined by said clock offset estimation means (1) to adjust the own cycle timer (3) to reduce its timing error.

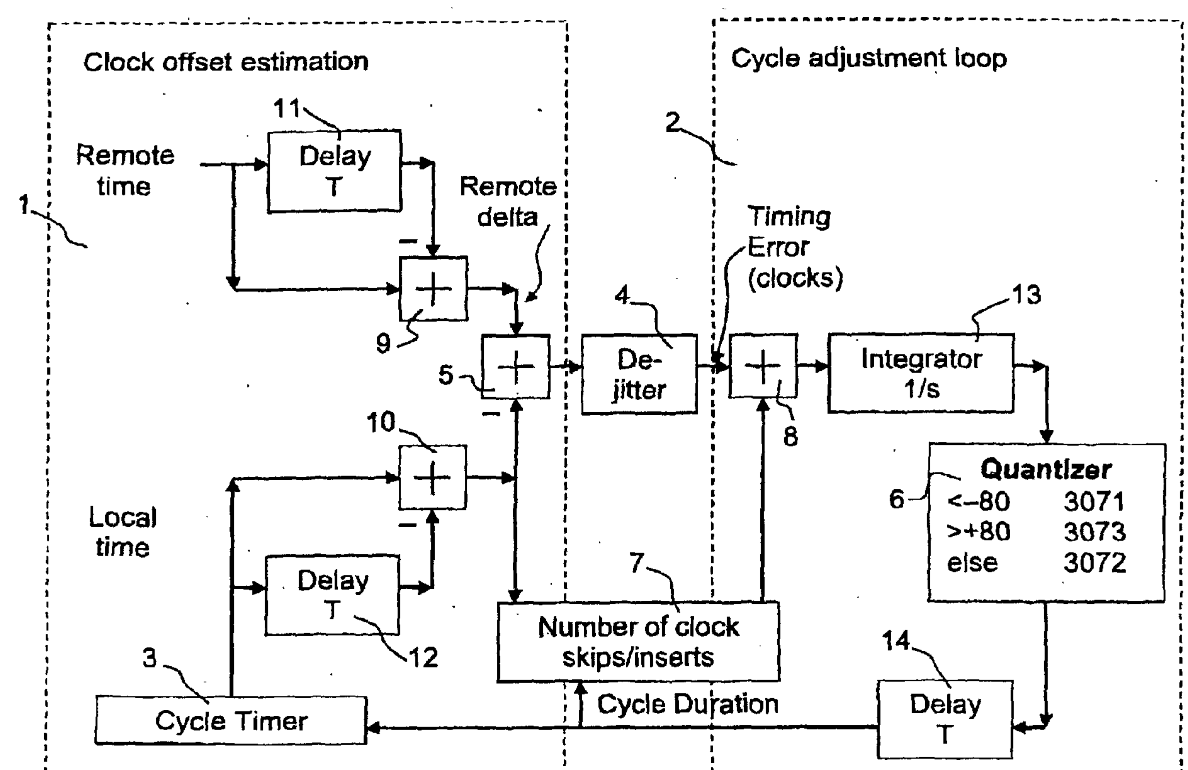

Figure 3

Printed by Jouve, 75001 PARIS (FR)

Description

[0001] The present invention relates to a method to perform a cycle synchronization between interconnected sub-networks and a cycle synchronizator adapted to perform said method.

[0002] It is known to interconnect sub-networks, e. g. with long delay bi-directional connections to extend a network to a wider area. In particular, this technique is used to interconnect several IEEE 1394 serial buses to extend an IEEE 1394 network, e. g. through a whole house. The basic topology of such a connection is shown in Fig. 1. A first interface 20 is part of a first IEEE 1394 serial bus 21 which might consist of a number of IEEE 1394 nodes. A second interface 22 is part of a second IEEE 1394 serial bus 23 which might comprise another number of IEEE 1394 nodes. The first interface 21 and the second interface 22 are connected via a long delay bi-directional connection 24 which might be, but is not restricted to a coax cable medium.

[0003] Independent IEEE 1394 buses must be synchronized to have the same cycle rate. In particular, the IEEE 1394 standard mandates that for opened isochronous channels an isochronous packet is sent in every isochronous cycle. To ensure that isochronous transfers between the interconnected IEEE 1394 buses work, it must be ensured that all buses have the same frequency of isochronous cycles.

[0004] Therefore, it is the object underlying the present invention to provide a method to perform a cycle synchronization between interconnected sub-networks and a cycle synchronizator adapted to perform said method.

[0005] The method according to the present invention is defined in independent claim 1 and the cycle synchronizator according to present invention is defined in independent claim 12. Preferred embodiments thereof are respectively defined in the dependent subclaims.

[0006] The method to perform a cycle synchronization between interconnected sub-networks according to the present invention is characterized in that a reference node connected to one of the sub-networks transmits a respective cycle time information to cycle masters of all other sub-networks at recurring time instants, and the cycle masters of all other sub-networks adjust their cycle time accordingly.

[0007] Therewith, the present invention offers a method to synchronize several interconnected sub-networks which is independent of the connection between the sub-networks, since with the transmission of cycle time information of a reference node no relying on a clock frequency used for the transmission through the connection through sub-networks is necessary. After reception of the cycle time information each cycle master of the other sub-networks can adjust their cycle time accordingly so that in turn the cycle frequency in an IEEE 1394 serial bus connected to a respective cycle gets adjusted. Therefore, in a network with N sub-networks N-1 cycle masters are required to adjust their cycle time and the remaining sub-network has to comprise the reference node transmitting its time information to the N-1 cycle masters of the other sub-networks. Preferably, the reference node and the cycle masters are arranged within a respective interface of the sub-network which is connected to the interconnection of all sub-networks.

[0008] According to the present invention an adjustment of the cycle time within a cycle master might be performed by the following steps: Determining a first time interval in-between two receptions of cycle time information from the reference node with an own clock, determining a second time interval in-between corresponding transmission of cycle time information from the reference node on basis of the received cycle time information, comparing the first and second time intervals and adjusting the own cycle time according to the comparison result. Therefore, a large scale integration is possible.

[0009] Further, the comparison of the first and the second time intervals according to the present invention might consider a preceding adjustment of the own cycle time, the adjustment of the own cycle time within a cycle master might be performed in a step-wise manner and/or the adjustment of the own cycle time within a cycle master might be performed by adjusting a local number of clocks within one cycle.

[0010] In particular, in the latter case the adjustment of the own cycle time within a cycle master is performed by setting the local number of clocks equal to an ideal number of clocks of one cycle in case the first time interval and the second time interval are identical, smaller than an ideal number of clocks of one cycle in case the first time interval is smaller than the second time interval and larger than an ideal number of clocks in case the first time interval is larger than the second time interval. In particular, these features enable a very easy and therefore reliable method to perform the cycle synchronization between interconnected sub-networks according to the present invention which is independent from the transmission method used in-between the sub-networks.

[0011] The stepwidth of setting the local number of clocks smaller or larger than the ideal number of clocks might be determined according to the difference of the first and second time intervals. In this case it is possible to determine how fast the sychronization should be achieved and/or to consider smaller and larger deviations of the cycle timers within the cycle masters.

[0012] According to the present invention preferably the cycle time information transmitted by the reference node is a content of its cycle time register. In this case the adjustment of the own cycle time within a cycle master is preferably performed by adjusting the average difference between a time interval of two transmissions of cycle time information of the reference node which is determined by subtracting two succeeding received contents of the cycle time register of the reference node

and a time interval of two samplings of the own cycle timer which is determined by subtracting two succeeding sampled contents of the own cycle time register plus a corrective difference to be zero. Of course, also other than two succeeding transmissions could be used, but in this case the hardware design to realize a cycle synchronizator according to the present invention leads to an increased cost. Further preferably, the corrective difference corresponds to the preceding adjustment.

[0013] Further preferably, according to the present invention the recurring time instants are determined to a regular time interval with a small variation.

[0014] The cycle synchronizator according to the present invention is therefore characterized by a clock offset estimation means to determine a timing error of an own cycle timer, and a cycle adjustment loop receiving the timing error determined by said clock offset estimation means to adjust the own cycle timer to reduce its timing error. Preferably, a de-jitter filter is arranged in-between the clock offset estimation means and the cycle adjustment loop to filter said determined timing error.

[0015] Therefore, in case the present invention is applied to a distributed IEEE 1394 network, i. e. several IEEE 1394 serial buses which are regarded as sub-networks are interconnected, e. g. by a long delay, bi-directional connection provides advantages in that the cycle synchronization is based on free-running oscillators of the cycle masters and standard IEEE 1394 physical interfaces can be used, since the cycle synchronization is based on a timing error of the own cycle timer which can be determined on basis of the transmission of cycle time information of a reference node in the network. Additionally, the reference node does not need to be a cycle master, i. e. the reference node can be predetermined.

[0016] Further features and advantages of the present invention will be apparent from the following detailed description of an exemplary embodiment thereof taken in conjunction with the accompanying drawings, in which

Fig. 1 shows an overview of a simple long delay IEEE 1394 network,

Fig. 2 shows a timing diagram of a first preferred embodiment according to the present invention, and

Fig. 3 shows a phase locked loop for cycle synchronization according to a preferred embodiment of the present invention.

[0017] The following preferred embodiment of the present invention is adapted to the IEEE 1394 standard. However, as mentioned above, the present invention is not restricted thereto.

[0018] Every IEEE 1394 node maintains cycle time information. This is basically a register that is incremented by a local, free-running clock of 24.576 MHz or integer multiples of that. According to the present invention this cycle time information is transmitted at regular instants via the interconnection of several sub-networks, in case of the example shown in Fig. 1 via the long delay bi-directional connection 24. The basic assumption of this method is that transmission of the cycle occurs at recurring time instants, preferably regular intervals, e. g. every 10 ms. Further, the exact value of that interval is not important since the exact value can be recovered from the difference of two transmitted samples of the cycle time register and the corresponding time stamps of the receiver will be sampled at the instant when the transmitted samples are received.

[0019] Fig. 2 shows an example of timing of the transmission and reception of the cycle time. The node which has been chosen to be the reference node transmits the time at least to all other nodes comprising a cycle master. As mentioned above, the reference node is not required to be the cycle master within its connected IEEE 1394 sub-network. As shown in Fig. 2, the reference node samples its local cycle time register at regular instants, i. e. at a first transmission time t_0, a second transmission time t_3, and a third transmission time t_5 at which the contents of the cycle time register are respectively transmitted. It it also shown in Fig. 2 that the second transmission time t_3, which is an actual transmission time, differs from an ideal second transmission time t_2 by a time difference $t_{jitter1}$. After a respective transmission of the contents of the cycle time register these contents are received at a first reception time t_1, a second reception time t_4, and a third reception time t_6. Similar to the case of the transmission it is shown in Fig. 2 that the actual reception of the transmitted cycle time register content at the second reception time t_4 differs from an ideal reception thereof. The difference in-between the ideal and the later actual second reception time is labelled with $t_{jitter2}$. A difference in-between the first and second actual transmission times is determined to Δt_2 and in-between the second and third actual transmission times to $\Delta t_2'$. A difference in-between the first and second actual reception times is determined to Δt_1 and in-between the second and third actual reception times to $\Delta t_1'$.

[0020] To allow for significant jitter to occur both on the transmitter and on the receiver side according to the present invention an optional filtering can be performed which limits the cycle length adjustment range to +/- 1 clock and/or which uses a de-jitter filter.

[0021] After transmission, the receiving node samples its own local cycle timer at the instant when it receives the remote cycle time information. In the standard IEEE 1394 node, one cycle has a duration of 3072 clocks of a 24,576 MHz oscillator. According to the preferred embodiment of the present invention shown and described in the following, a cycle timer is used where the duration of the cycle can be adjusted to 3071, 3072 or 3073 clocks. However, a variable duration might also

be implemented. The information of the remote and local cycle time registers is used to adjust the local number of clocks per cycle.

[0022] According to the preferred embodiment of the present invention a special phase locked loop as shown in Fig. 3 is used to achieve the synchronization.

[0023] The cycle synchronizator shown in Fig. 3 comprises a clock offset estimation means to determine a timing error in clocks which is supplied to a cycle adjustment loop 2 preferably, as shown in Fig. 3, via a de-jitter filter 4. The cycle adjustment loop 2 in turn determines a new cycle duration which is supplied back to the clock offset estimation means 1.

[0024] In particular, the clock offset estimation means 1 receives the remote time which is supplied directly as minuent to a first adder 9 and via a first delay element 11 as subtrahend to the first adder 9. The first delay element 11 holds the preceding sample of the remote time, i. e. shows a FIFO-behaviour with a storage capacity of one sample. Therefore, the first adder 9 outputs a remote time delta, i. e. the time difference of the time in-between two samples of the time register of the reference node. This remote time delta is input as minuent to a second adder 5. Further, the clock offset estimation means 1 comprises the local cycle timer 3 of the cycle master. The local time output therefrom is input as minuent to a third adder 10 and via a second delay element 12 also as subtrahent to the third adder 10. The second delay element 12 shows the same delay T as the first delay element 11. Therefore, the third adder 10 outputs a local time delta corresponding in time to the remote time delta output by the first adder 9. This local time delta is input as subtrahent to the second adder 5 which outputs the timing error in clocks to the de-jitter filter 4 which inputs the filtered timing error in clocks to the cycle adjustment loop 2. Further, the local time delta output from the third adder 10 is input to a controller 7 which determines the number clock skips/inserts necessary on basis of an arithmetic operation subtracting the duration of a cycle in clocks for this period of time from that of an ideal cycle and multiplying the resulting difference by the quotient of the number of clocks between the previous sampling instant and this sampling instant with the duration of a cycle in clocks for this period of time.

[0025] The cycle adjustment loop 2 comprises a fourth adder receiving the timing error in clocks from de-jitter filter 4 as a first summand and the number of clock skips/inserts determined by the controller 7 as second summand to build their sum. This sum is supplied to an integrator 13 which outputs its integration result to a quantizer 6. The quantizer 6 determines whether the next cycle of the cycle timer 3 within the clock offset estimation means 1 should comprise 3071, 3072 or 3073 clocks. In case the integration result of the integrator 13 is smaller than -80 then the next cycle should comprise 3071 clocks, in case the integration result is bigger than 80 then the next cycle should comprise 3073 clocks and in case the output result of the integrator 13 equals to 80 the cycle should comprise 3072 clocks. This comparison introduces an hysteresis into the loop so that there are usually only differences of one clock in suceeding cycles, i. e. that there is usually no jump from 3071 to 3073, but either between 3072 and 3073 or between 3071 and 3072 clocks per cycle. Therefore, also another value than 80 cycles which equal to 10 ms might be used. The number of clocks output by the quantizer 6 is input to a third delay element 14 which also has the same delay T as the first delay element 11. The cycle duration output by the third delay element 14 is supplied to the controller 7 which determines the number of clock skips/inserts and to the cycle timer 13.

[0026] As mentioned above, the delay T of the first to third delay elements 11, 12, 14 are not fixed but depend on the reception of a transmitted remote time. Also, the delay T within the delay elements does not indicate a fixed or preset time, but that the sample and hold operation performed by the delay element is performed by all three delay elements simultaneously.

[0027] The phase locked loop for a cycle synchronization according to the preferred embodiment of the present invention shown in Fig. 3 adjusts the average difference between the remote time interval which is measured with the remote clock and the local time interval which is measured with the local clock plus a corrective difference to be zero.

[0028] Since without jitter or disturbances the delay of the transmission path between reference and cycle synchronizator is constant, the method according to the present invention uses exactly the time interval for the local and remote measurement. Since the respective oscillators used for the respective measurement might differ slightly with respect to their oscillation frequency, i. e. according to the IEEE 1394 standard +/- 100 ppm are allowed, these measurements of local and remote time intervals do not give exactly the same number of clocks. The cycle synchronizator according to the present invention extracts the number of cycles n_cycles that have elapsed in the respective time interval and depending on the current cycle duration, the corrective number of clocks is set to be either +n_cycles, 0, or -n_cycles. Corrective values of -1,0 + 1 per 3072 clocks as explained above is equivalent to an adjustment range of +/- 166/3072 = +/- 325 ppm. Also larger corrective values might be used which - on the other hand - lead to higher local jitter and are therefore not preferred. Therefore, in the long run, the remote and local number of cycles are equalized.

[0029] As shown in Fig. 3 it is advantageous to insert a de-jitter filter 4 before the cycle timer adjustment loop. A suitable filter is a lowpass filter, but other filters, e. g. a running mean or a time-adaptive lowpass may also be used. By choosing a suitably high time constant in that filter which is independent from the clock synchronization loop the jitter can be eliminated.

[0030] Since the IEEE 1394 serial bus is a self-configuring bus, it is necessary that the network reference

node is automatically determined after each network reconfiguration, e. g. after the addition or removal of nodes.

[0031] Therefore, according to the present invention the oscillator is not adjusted, but the number of clocks within one cycle. Therefore, a free-running oscillator can be used instead of a voltage controlled oscillator. This feature enables the integration of the cycle synchronization according to the present invention on a single chip. Further, as mentioned above, the present invention performs the cycle synchronization independently of the connecting channel in-between the different sub-networks, i. e. IEEE 1394 serial buses which basically need only slight modifications in that the cycle synchronizator according to the present invention has to be included into a respective cycle master of a sub-network. Further, the connection network needs no master clock, since one of the sub-networks serves as reference.

Claims

1. Method to perform a cycle synchronization between interconnected sub-networks, **characterized in that**

- a reference node connected to one of the sub-networks transmits a respective cycle time information to cycle masters of all other sub-networks at recurring time instants, and
- the cycle masters of all other sub-networks adjust their cycle time accordingly.

2. Method according to claim 1, **characterized in that** an adjustment of the cycle time within a cycle master is performed by the following steps:

- determining a first time interval (Δt_1, $\Delta t_1'$) in-between two receptions of cycle time information from the reference node with an own clock,
- determining a second time interval (Δt_2, $\Delta t_2'$) in-between two corresponding transmissions of cycle time information from the reference node on basis of the received cycle time information,
- comparing the first time interval (Δt_1, $\Delta t_1'$) and the second time interval (Δt_2, $\Delta t_2'$), and
- adjusting the own cycle length according to the comparison result.

3. Method according to claim 2, **characterized in that** the comparison of the first time interval (Δt_1, $\Delta t_1'$) and the second time interval (Δt_2, $\Delta t_2'$) considers a preceding adjustment of the own cycle length.

4. Method according to claim 2 or 3, **characterized in that** the adjustment of the own cycle length within a cycle master is performed in a step-wise manner.

5. Method according to claim 2, 3 or 4, **characterized in that** the adjustment of the own cycle length within a cycle master is performed by adjusting a local number of clocks within one cycle.

6. Method according to claim 5, **characterized in that** the adjustment of the own cycle length within a cycle master is performed by setting the local number of clocks

- equal to an ideal number of clocks of one cycle in case the first time interval (Δt_1, $\Delta t_1'$) and the second time interval (Δt_2, $\Delta t_2'$) are identical,
- smaller than an ideal number of clocks of one cycle in case the first time interval (Δt_1, $\Delta t_1'$) is smaller than the second time interval (Δt_2, $\Delta t_2'$), and
- larger than an ideal number of clocks in case the first time interval (Δt_1, $\Delta t_1'$) is larger than the second time interval (Δt_2, $\Delta t_2'$).

7. Method according to claim 6, **characterized in that** a step-width to adjust the own cycle timer within a cycle master is set according to the difference of the first time interval (Δt_1, $\Delta t_1'$) and the second time interval (Δt_2, $\Delta t_2'$).

8. Method according to anyone of the preceding claims, **characterized in that** the cycle time information transmitted by the reference node is a content of its cycle time register.

9. Method according to claim 8, **characterized in that** the adjustment of the own cycle time within a cycle master is performed by adjusting the average difference between a time interval of two transmissions of cycle time information of the reference node which is determined by subtracting two succeeding received contents of the cycle time register of the reference node and a time interval of two samplings of the own cycle timer which is determined by subtracting two succeeding sampled contents of the own cycle time register plus a corrective difference to be zero.

10. Method according to claim 9, **characterized in that** the corrective difference corresponds to the preceding adjustment.

11. Method according to anyone of the preceding claims, **characterized in that** the recurring time instants are determined according to a regular time interval with a small variation.

12. Cycle synchronizator, **characterized by**

- a clock offset estimation means (1) to determine a timing error of an own cycle timer (3),

and

- a cycle adjustment loop (2) receiving the timing error determined by said clock offset estimation means (1) to adjust the own cycle timer (3) to reduce its timing error.

13. Cycle synchronizator accordingto claim 12, **characterized by** a de-jitter filter (4) arranged in-between the clock offset estimation means (1) and the cycle adjustment loop (2) to filter said determined timing error.

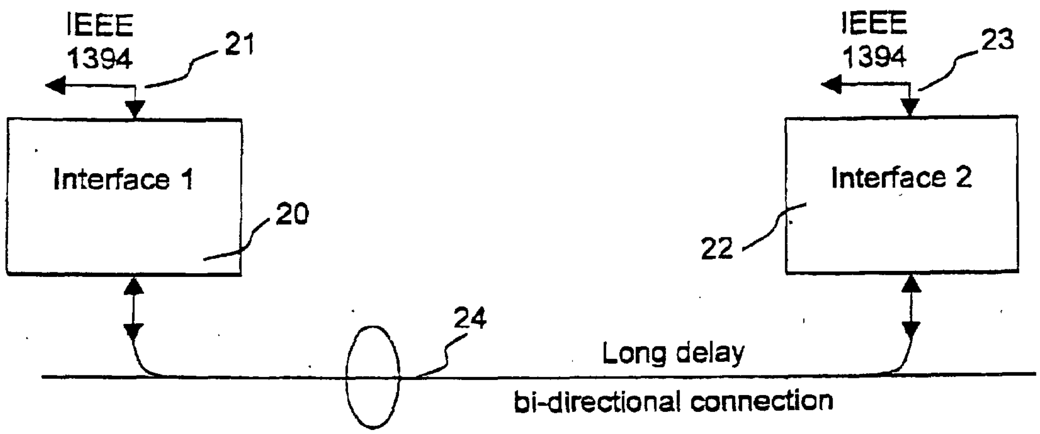

Figure 1

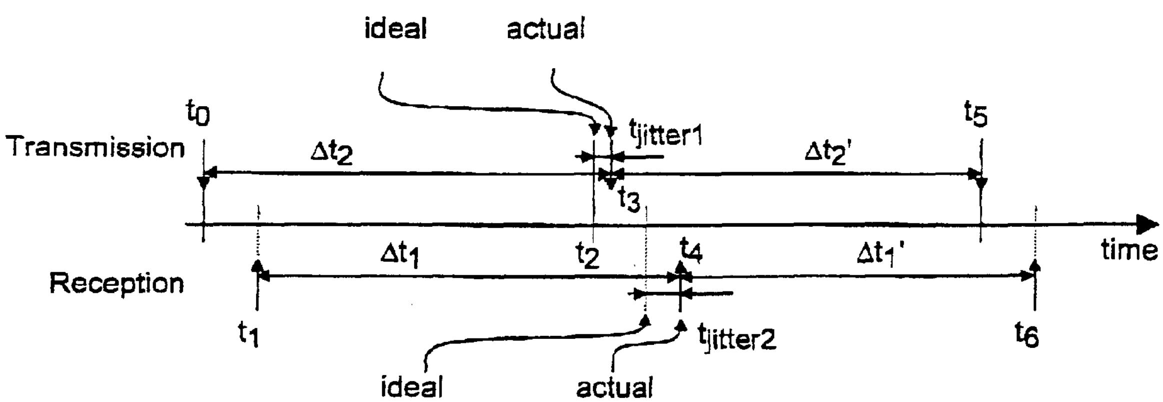

Figure 2

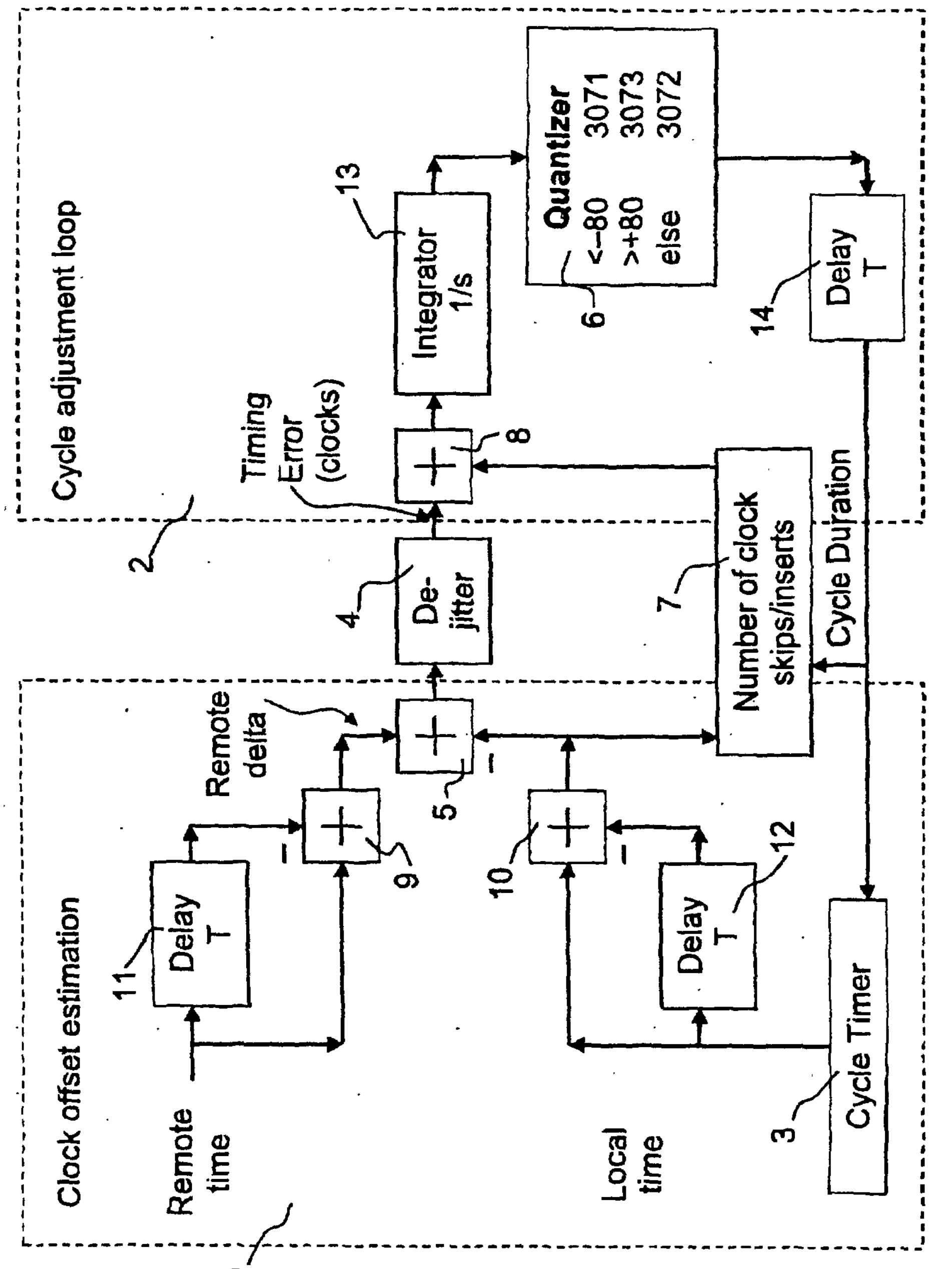
Clock offset estimation
Cycle adjustment loop
Remote time
Local time
Delay T
Delay T
Delay T
Remote delta
Timing Error (clocks)
De-jitter
Integrator 1/s
Quantizer
<-80 3071
>+80 3073
else 3072
Number of clock skips/inserts
Cycle Duration
Cycle Timer
1
2
3
4
5
6
7
8
9
10
11
12
13
14

Figure 3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 12 2026

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	EP 1 009 116 A (SONY CORP) 14 June 2000 (2000-06-14)	1,8	H04J3/06 G06F1/14
Y	* column 1, paragraph 4 - column 2, paragraph 8 * * column 7, paragraph 35 * * column 16, paragraph 81 - column 18, paragraph 93 *	2-5,9-11	
A	* figures 2,9,10,13-17 * ---	6,7,12, 13	
Y	EP 0 722 233 A (HEWLETT PACKARD CO) 17 July 1996 (1996-07-17)	2-5,9-11	
A	* abstract * * column 8, line 53 - column 9, line 45 * * figure 11 * ---	13	
X	US 5 608 731 A (UPP DANIEL C ET AL) 4 March 1997 (1997-03-04) * abstract * * column 3, line 38 - column 4, line 18 * * figure 2 * ---	12,13	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)
X	US 6 032 261 A (HULYALKAR SAMIR N) 29 February 2000 (2000-02-29)	1	H04J G06F H04N
A	* abstract * * column 2, line 51 - column 3, line 67 * * figures 3,4 * ---	8	
A	US 6 128 318 A (SATO TAKASHI) 3 October 2000 (2000-10-03) * abstract * * column 1 - column 2 * * figures 1-3 * --- -/--	1,12	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	5 March 2001	Fouasnon, O

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 12 2026

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	EP 0 942 556 A (SONY CORP) 15 September 1999 (1999-09-15) * abstract * * paragraphs '0027!,'0028!,'0035!,'0039!,'0046!-'0048! * * figures 1-5 * -----	1,12	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	5 March 2001	Fouasnon, O

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 00 12 2026

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

05-03-2001

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 1009116 A	14-06-2000	JP 2000165364 A	16-06-2000
EP 0722233 A	17-07-1996	US 5566180 A	15-10-1996
		JP 8221336 A	30-08-1996
US 5608731 A	04-03-1997	CA 2219118 A	03-10-1996
		EP 0872056 A	21-10-1998
		WO 9631028 A	03-10-1996
US 6032261 A	29-02-2000	CN 1254426 T	24-05-2000
		EP 0961977 A	08-12-1999
		WO 9935587 A	15-07-1999
US 6128318 A	03-10-2000	EP 0972371 A	19-01-2000
		WO 9938287 A	29-07-1999
EP 0942556 A	15-09-1999	JP 11261579 A	24-09-1999
		AU 1858899 A	23-09-1999

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82